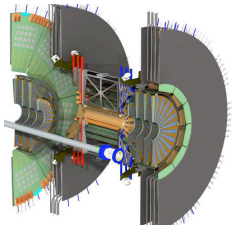
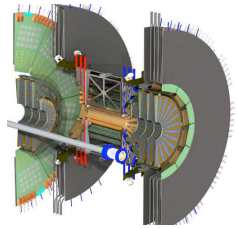


FVTX Monthly/Quarterly Report
March 25, 2009

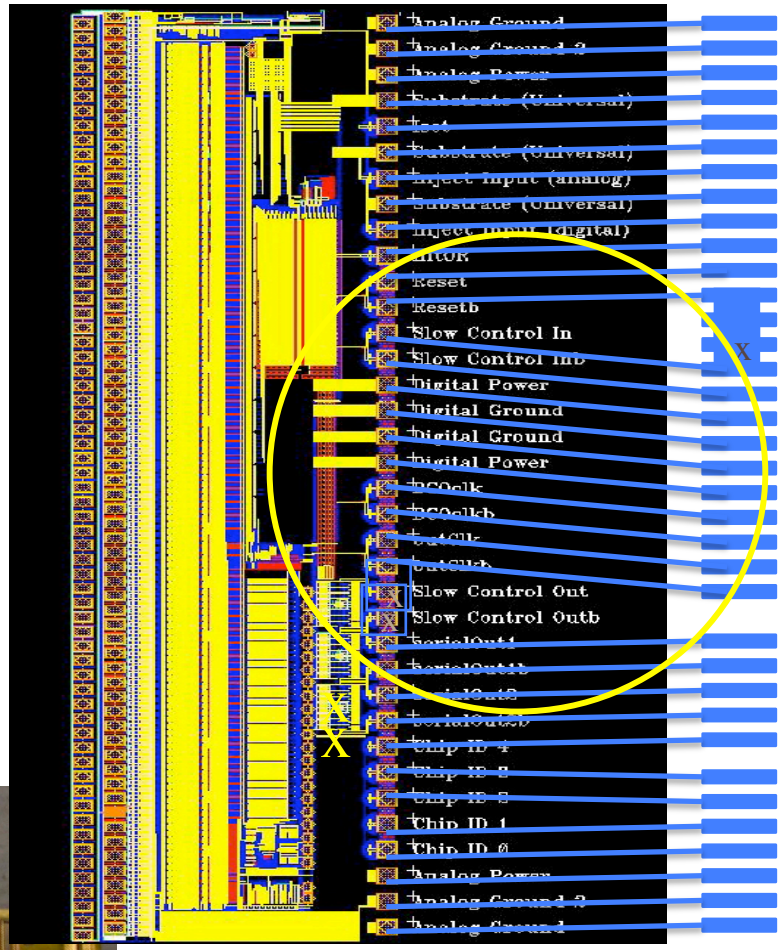
Melynda Brooks, LANL

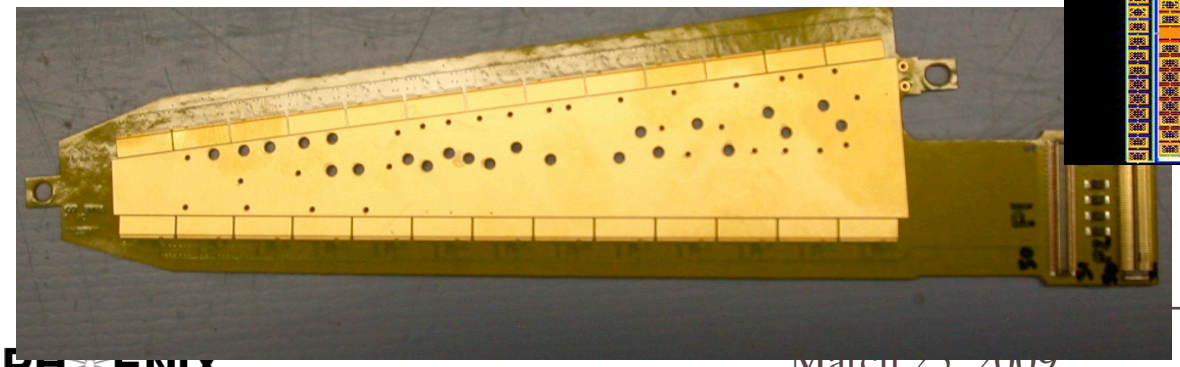
HDI and Assembly Status and Lessons Learned



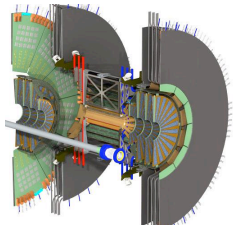
- Kapton HDI in hand
- PCB HDI in hand

- Kapton HDI underwent tests at LANL of schematics (passed) and clock distribution tests (good transmission with expected capacitance added onto lines).
- Gave FNAL SiDet go-ahead to bond one chip to HDI for testing (March 16)
- FPHX→HDI bonding pattern had to take into account change in FPHX bond pads between rev_final and rev_final-1
- FVTX personnel traveled to FNAL for testing, assembly oversight

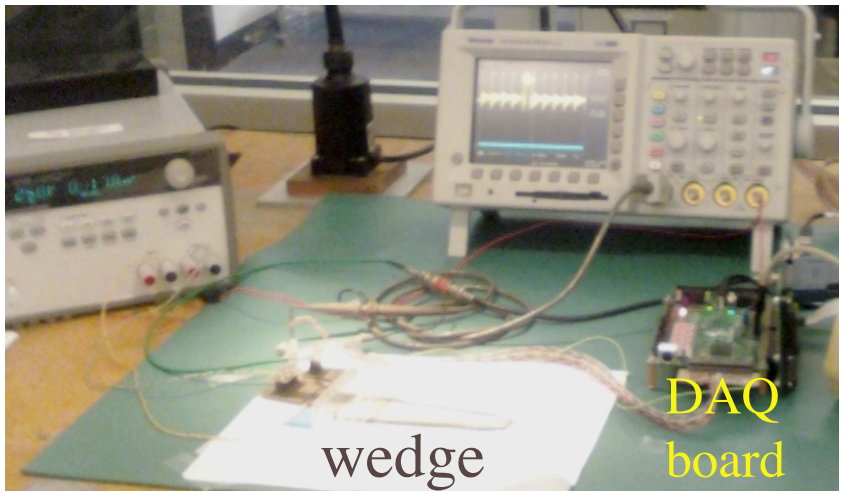


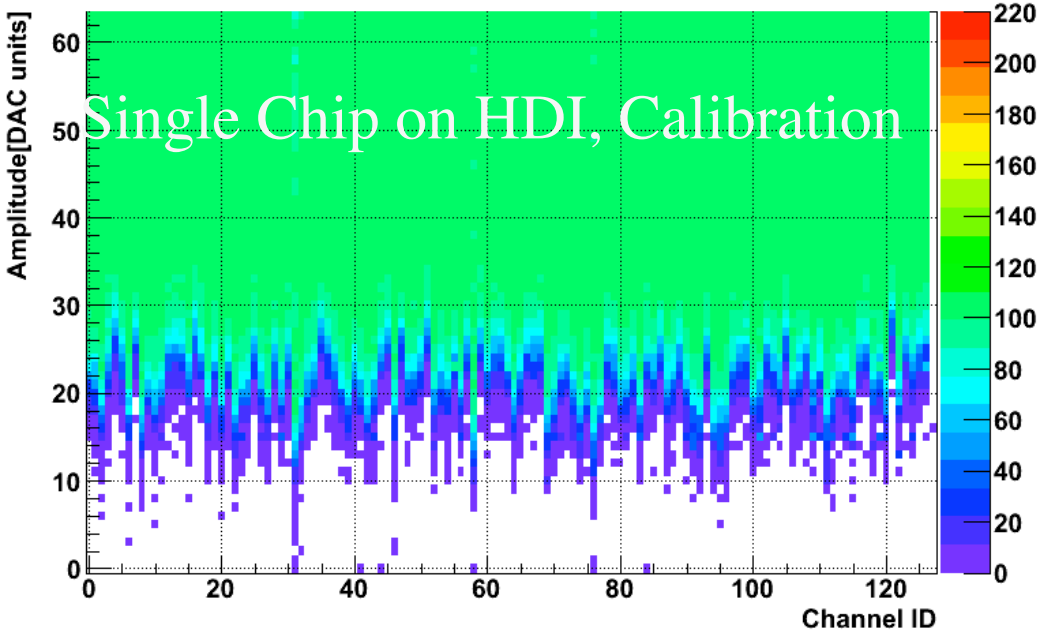


FPHX Wedge Test Results, Lessons Learned

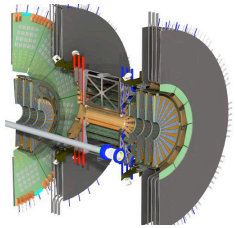


- Single chip bonded to HDI
- HDI→DAQ interconnect made for single-chip readout
- Verified rest of chip worked
- Verified slow control download worked
- Connected to calibration system and took data
- Kapton interconnection difficult without PCB board interface (in progress)
- Test setup somewhat noisy, but verified calibration data looked reasonable
- Gave go-ahead to bond 13 chips (1/2 wedge) and sensor to HDI

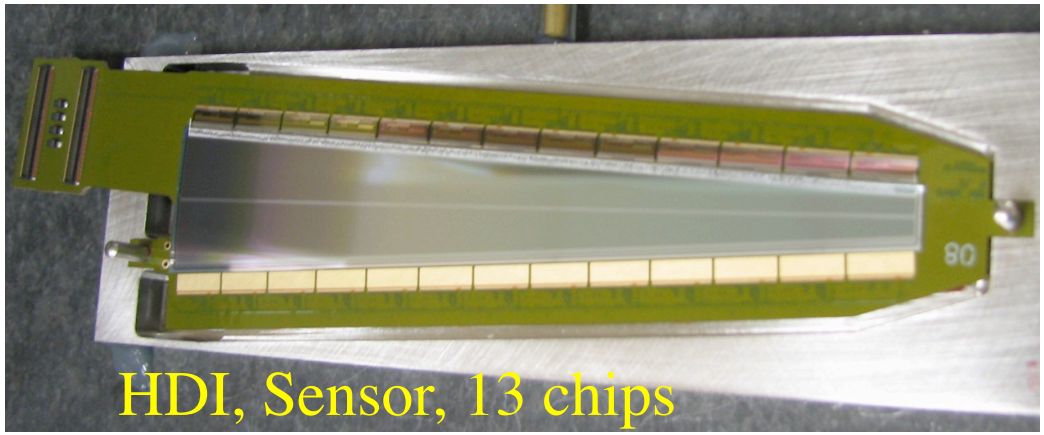


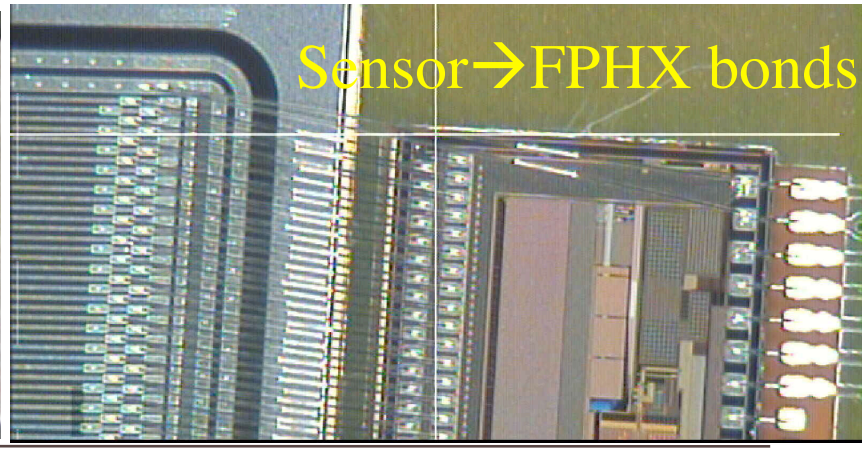


FPHX Wedge Assembly, Lessons Learned

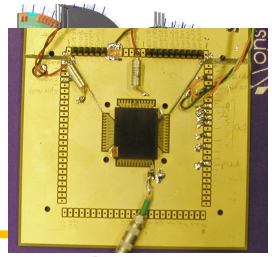


- 13 chips and silicon bonded to HDI, wire bonds applied and encapsulated
- Shipping to LANL, will test:
  - Read 1 chip with sensor
  - Read 1 chip with other 12 chips “active”
  - Read 13 chips at same time
  - Optimize noise, check integrity of data, etc.
- Better HDI->DAQ interconnect underway
- Assembly fixtures mostly worked (well) but mismatch between jig and HDI in chip spacing meant chips were laid by hand. Will modify or re-make jig for production.
- Sensor bias-ring pad on HDI missing – made 4 bonds from sensor to FPHX analog ground directly instead



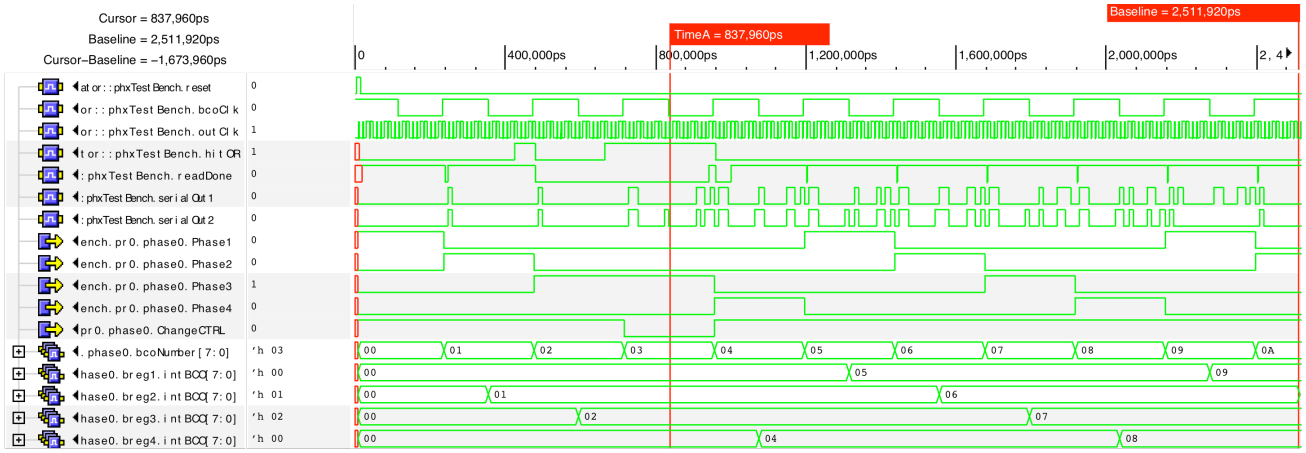


FPHX Design work



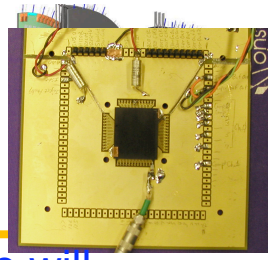
Met with FPHX designers at FNAL March 18 to discuss FPHX redesign work:

- Jim Hoff, digital design engineer had found some time in the previous week to look at digital issues (wrong BCO clock on some events, desire to select between different readout lines, wanted to add a bit to the data word)
- ALL DIGITAL REDESIGN WORK COMPLETED.
- Simulations of each fix completed, for digital end of chip
- Tom Zimmerman, analog design engineer estimates he needs <1 week to carry out the analog redesign work
- May MOSIS submission should be no issue, but 2 months past MP
- They will expect a full FPHX review prior to submission



Simulated, digital fix to BCO storage

FPHX Tests suggested from FPHX Review



- Look at large pulse recovery – Tom Zimmerman investigated previously, we will repeat
- Look at sensitivity to power supply voltage – Just need to do
- Should complete tests using internal pulser (FNAL tested but we did not)
- Should try running at real PHENIX beam clock (9.4 MHz as opposed to 10.0 MHz)

Partially Done (see last bullet) – no issue with short-term data readout

- Should vary cable lengths carrying LVDS and check performance - Just need to do
- Measure sensitivity to phase relation between beam clock and read clock

Done – no issue with data readout

- Check the reset timing requirements in more detail: we know we have to issue reset on proper edge; how much out of phase can we be and it still works?

Done – reset can be out of time up to ~15 ns and still operate fine

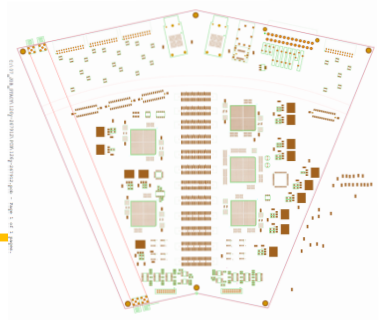
- Check performance of chip when data output is active – suggest reading calibration data from one channel while a “noisy” channel is also unmasked

Done – no issue with data readout

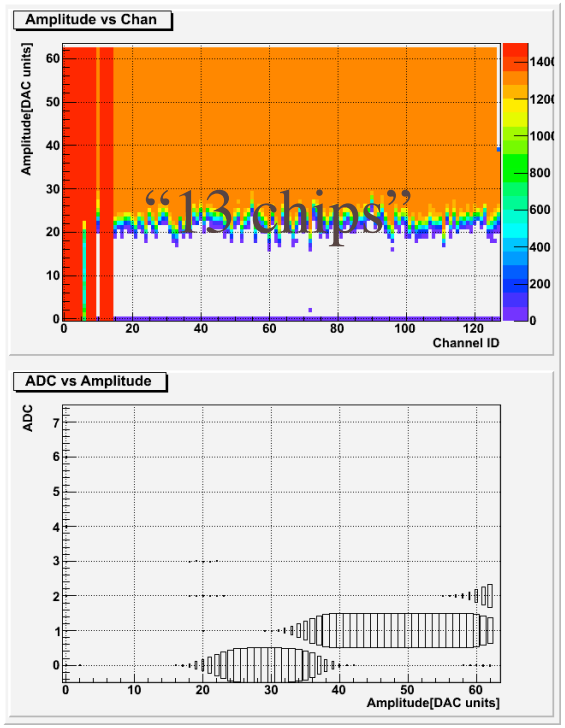
- Try some longer burn-in tests – many hours or days

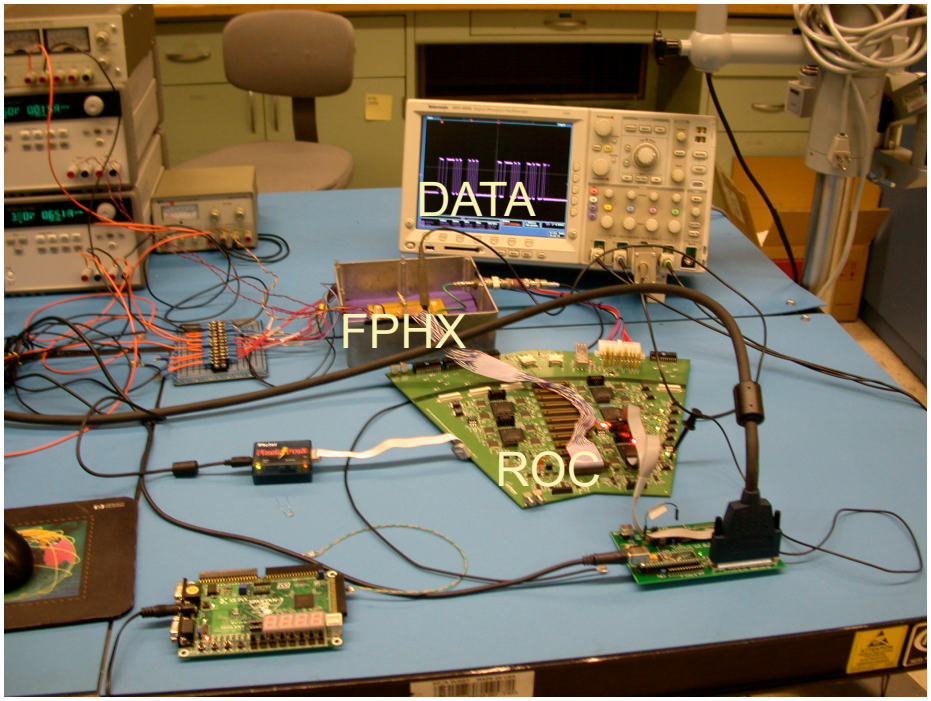
In progress – issues with 9.4MHz clock, probably just because of implementation. 10 MHz looks good.

FVTX Technical Status - DAQ



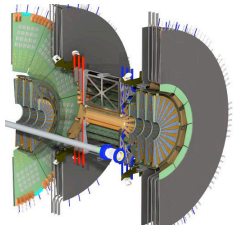
- ROC board will be used for Wedge Test
- FEM design in progress – FPGA, interconnect pinouts “frozen”





ROC board communicating with single FPHX chip, oscilloscope and computer readout.

Cost & Schedule



No new cost updates since last monthly report

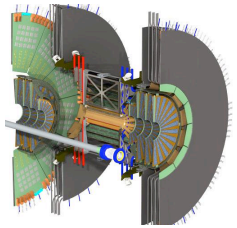
- Contingency is approximately what it was in MP

Schedule

- Critical path items are wedge testing, FPHX redesign work
- FPHX redesign and resubmission can be in place by end of May (would take 2 months out of 5 months of float in critical path)
- Wedge testing time uncertain until we get further into tests
- Engineers/reviewers know we want to discuss 2nd MOSIS versus engineering run before May

- Coming Milestones:
  - Sensor procurement complete (Q309) – may delay, not critical path
  - Review FEM and ROC (Q309) – may delay, not critical path
  - Wedge assembly test complete (Q309)

Summary



Wedge Assembly Tests

- Fully assembly tests about to begin
- Results will determine project schedule

HDI

- Some (minor) redesign known to properly bond to FPHX chips
- Final design determined by results of wedge test.

Wedge tests

- Expect wedge assembly to begin soon
- SiDet tested assembly process, small mods to chip placement especially

ROC/FEM

- Roc prototype testing underway
- Prototype ROC will be used for wedge tests
- FEM still behind schedule, but not on critical path